SpinalHDL, VexRiscv, SaxonSoc
Whoami

- Charles Papon
- Hardware/Software background
- Main dev behind
  - SpinalHDL, VexRiscv, SaxonSoc
FPGA to deploy hardware

• Pro
  - Affordability (dev kit ~30$-200$, low initial cost)
  - Iterate in a few minutes

• Their limitations:
  - Large volume => high cost
  - Speed
  - Design size
  - Only digital
  - ...
SpinalHDL

- HDL => Hardware description language
- A „modern“ alternative to VHDL/Verilog/SystemVerilog
- Technically it is a Scala iDSL
- Also implement some modules
  - DDR3 controller
  - Ethernet controller
  - USB host controller (NLnet funded)
  - ...
- https://github.com/SpinalHDL/SpinalHDL
VexRiscv

- CPU targeted for FPGA deployement
  - RISC-V 32 bits
  - Multi core
  - Memory coherency
  - Can run upstream linux
  - 64 bits FPU, AES (NLnet funded)
- Allow peoples to extends it
- Avoid FPGA vendor’s IP creep
- https://github.com/SpinalHDL/VexRiscv
SaxonSoc

- Framework to compose SoC
- For instance on ArtyA7 35T
  - 2 VexRiscv ~100 Mhz
  - Shared FPU
  - DDR3, Sdcard
  - Ethernet, USB host,
  - Video/Audio output
- https://github.com/SpinalHDL/SaxonSoc/tree/dev-0.3/bsp/digilent/ArtyA7SmpLinux
- Linux
- Buildroot
- x11
- mpg123
- Dillo
- USB boot
- ...